AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1-129.   (canceled)

1   130. (original) An integrated circuit device comprising:

2   a circuit to convert an input value into a search value;

3   a first storage including content addressable memory (CAM) cells, compare lines

4   coupled to columns of the CAM cells and match lines coupled to rows of the

5   CAM cells, the compare lines being coupled to receive the search value;

6   a second storage coupled to the match lines of the first storage; and

7   a compare circuit coupled to an output of the second storage and coupled to receive

8   the input value.

1   131. (original) The integrated circuit device of claim 130 wherein the second storage

2   comprises an array of static random access memory (SRAM) cells.

1   132. (original) The integrated circuit device of claim 130 wherein the second storage

2   comprises an array of dynamic random access memory (DRAM) cells.

1   133. (original) The integrated circuit device of claim 130 wherein each of the CAM cells

2   comprises a compare circuit coupled to at least one of the compare lines and at least

3   one of the match lines.

1   134. (original) The integrated circuit device of claim 130 wherein the CAM cells within

2   a column of the CAM cells comprise respective compare circuits coupled to a

3   common pair of compare lines and to respective match lines.

1   135. (original) The integrated circuit device of claim 130 wherein the first storage further

2   includes word lines coupled to the rows of the CAM cells.

1   136. (original) The integrated circuit device of claim 130 further comprising a select

2   circuit having a first input port coupled to the word lines and a second input port

3   coupled to the match lines.

1   137. (original) The integrated circuit device of claim 136 wherein the second storage

2   comprises word lines coupled to an output of the select circuit.

1   138. (original) The integrated circuit device of claim 137 wherein the select circuit is

2   responsive to an operation select signal to select either a decoded row address

3   present on the word lines of the first storage or match signals present on the match

4   lines of the first storage to be output onto the word lines of the second storage.

1   139. (original) The integrated circuit device of claim 130 wherein the circuit to convert

2   the input value into a search value is a cyclic redundancy check (CRC) circuit that

3   generates a CRC value based on the input value, and wherein at least a portion of

4   the CRC value constitutes the search value.

1   140. (original) The integrated circuit device of claim 130 further comprising an interface

2   and an assembler circuit coupled to the interface, the assembler circuit being

3   configured to reorder selected bits within a value received via the interface to

4   generate the input value.

1   141. (original) The integrated circuit device of claim 130 wherein the circuit to convert

2   the input value comprises a mask circuit to mask selected bits in the input value.

1   142. (original) A content addressable memory (CAM) comprising:

2   a cyclic redundancy check (CRC) circuit to generate a CRC value; and

3   a CAM array having compare lines coupled to the CRC circuit to receive at least a

4   portion of the CRC value therefrom.

1   143. (original) The CAM of claim 142 wherein the CAM further comprises a mask

2   circuit to mask selected bits in the CRC value.

1   144. (original) The CAM of claim 143 further comprising a configuration circuit to store

2   a configuration value indicative of the selected bits to be masked within the CRC

3   value, the configuration circuit being coupled to the mask circuit to provide the

4   configuration value thereto.

1   145. (original) The CAM of claim 142 wherein the CRC value comprises N constituent

2   bits and wherein the at least a portion of the CRC value comprises M contiguous

3   bits of the CRC value, M being less than N.

1   146. (currently amended) A content addressable memory (CAM) comprising:

2   a CAM array including a plurality of CAM cells and a plurality of match lines

3   coupled to respective rows of the CAM cells;

4   a priority index table including a plurality of priority storage circuits coupled to

5   store respective priority values and coupled respectively to the plurality of

6   match lines; and

7   a multiplexer ~~having a first input coupled to receive a selected priority value from~~

8   ~~the priority index table, and a second input to receive a predetermined priority~~

9   ~~value,~~ to output a predetermined priority value in an operation to determine

10   where to store a first value within the CAM, and to output a selected priority

11   value from the priority index table in an operation to determine whether a

12   specified value is stored within the CAM.

1   147. (currently amended) The CAM of claim 146 wherein the priority values indicate

2   relative priorities of values stored within corresponding rows of the CAM cells.

1   148. (currently amended) The CAM of claim 146 wherein the ~~multiplexer is responsive~~

2   ~~to a select signal to output either the selected priority value or the predetermined~~

3   ~~priority value,~~ predetermined priority value indicates how filled the CAM array is.

149. (canceled)

1   150. (original) An integrated circuit device comprising:

2   means for converting an input value into a search value;

3   a first storage including means for generating a plurality of match signals that

4   indicate whether the search value matches respective values stored within the

5   first storage;

6   a second storage including means for outputting a value stored at a location within

7   the second storage indicated by the plurality of match signals; and

8   means for comparing the value output from the second storage with the input value.